Second Edition

Digital Electronics Drill

Solutions
Test Drill I
Test Drill II

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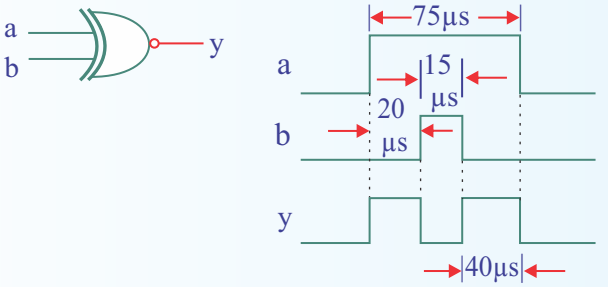
Digital Electronics Drill

Test Drill I

Q1.(a)



Q2. $x^2 + 2x + 3 + (x-2)^2 + 2(x-2) + 1 = 3 \times 16 + 6 \Rightarrow 2x^2 = 50$

$x = \pm 5$

Choose positive integer value of ***x=5.***

Q3.(a) The necessary and sufficient conditions for a function to be self dual are

(i)the function must be neutral .A function with equal number of max terms and min terms, is said to be neutral .

(ii) the function must not contain mutually exclusive terms .

The term $X = \bar{a}bc$ and the term $Y = a\bar{b}\bar{c}$ *obtained by complementing each literal, are said to be mutually exclusive .*

Only $f_1 = x$ and $f_4 = xy + \bar{x}y = y$ *satisfy these conditions.*

$f_1(x,y,z) = x = \sum(4,5,6,7)$ and $f_4(x,y,z) = y = \sum(2,3,6,7)$

Q4.(b) $f = (a\bar{b} + \bar{a}b)\bar{a} + \overline{(b+c)}a$

$= \bar{a}b + a\bar{b}\bar{c}$

Use K'map to get $\bar{f} = \bar{a}\,\bar{b} + ac + ab$

and $f = (a+b)(\bar{a}+\bar{c})(\bar{a}+\bar{b})$

	$\bar{b}\bar{c}$	$\bar{b}c$	bc	$b\bar{c}$
$\bar{a}$	0	0	1	1
a	1	0	0	0

Q5.(d) $T_{CLK} = 1/(20 \times 10^6) = 0.05\,\mu s = 50\,ns$

Let the counter state be defined as *dcba* with *d* as MSB .

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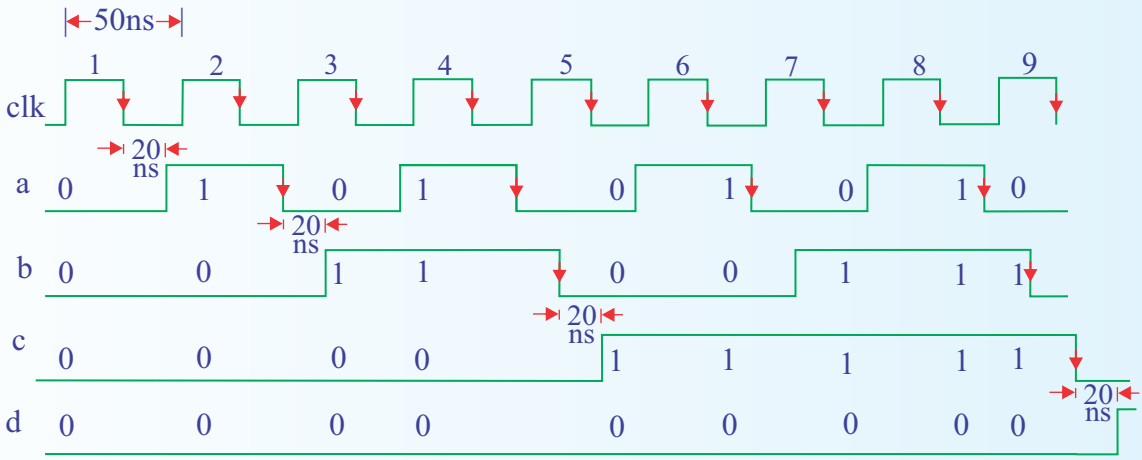
As demonstrated below, the counter counts normally from dcba = 0000 to 0111 until clock 7. At the 8th clock 'a' transits from 0 to 1 before 'd' transits from 0 to 1. There by , the counter skips the state dcba = 1000.



Q 6. $1\times R^1+1\times R^0+2(R+1)^1+3(R+1)^0=1\times R^2+0\times R^1+2R^0$

$R^2-3R-4=0\Rightarrow R=-1 \text{ or } 4;\ R \text{ can not be negative}.\ R=4$

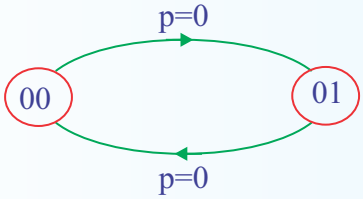
Q7.(d) $(26)_{16}\equiv(0010\ 0110)_2$
$(36)_{16}\equiv(0011\ 0110)_2$
$(A6)_{16}=(1010\ 0110)_2$
and $(37)_8=(011\ 111)_2$
The only negative number in 2's complement is
$(A6)_{16}=(1010\ 0110)_2\equiv-(90)_{10}$

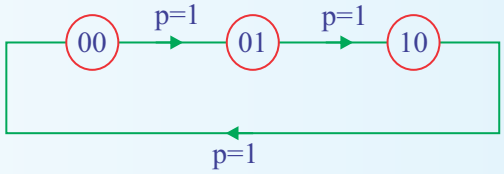
Q8.(c) The output of NOR gate is

$$x=\overline{(a+b+c)+\bar{a}bc}=\overline{a+b+c+bc}=\overline{a+b+c}=\bar{a}\ \bar{b}\ \bar{c}$$

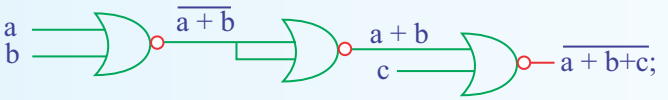
The input values a=b=c=0 will force the LED to glow.

Q9.(c) The machine is mod 2 counter for p = 0 and mod 3 counter for p=1. It is self starting in the sense that it goes to valid counting sequence for any initial state.





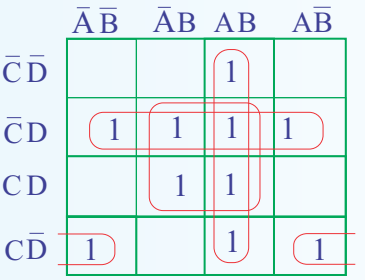
Q10.



$\lambda=3$

Q11.(b) Dividing a binary number by 6 ,is not possible by bit shifting.

Q12. Number of prime implicants = *4*.
The prime implicants are
.
AB , $\overline{C}D$, BD and $\overline{B}\,C\,\overline{D}$



Q13.(a) Inverting each bit and incrementing the result is equivalent to finding 2's complement.
$(-124)_{10} \equiv (1\,,0000100)_2$ in 2's complement
and 2's complement of $(1\,,0000100)_2$ is *0,1111100.*

Q14.(d)

clock cycle	1	2	3	4	5	6	7	8	9	10
X	1	1	1	0	0	0	1	1	1	0
state	S_0	S_1	S_2	S_3	S_0	S_0	S_0	S_1	S_2	S_3
M	0	0	0	1	0	0	0	0	0	1

$\Rightarrow$ *M=1 when input X has pattern '1110'*

Q15. The clock period must be > (D FF delay + maximum combinational circuit delay + D FF setup time)
$T_{CLK} > [15 + (35+10+25)+15]$
or $T_{CLK} > 100$ ps
CLK frequency $< [100\text{ ps}]^{-1} =$ *10 GHz*

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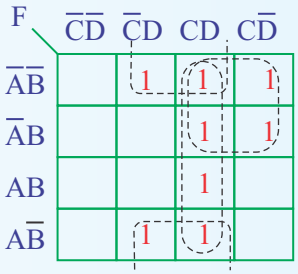
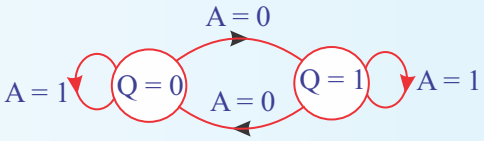
Q16. $1010 \oplus 0110 = 1100$
and $B = 01102 = 6_{10}$

Q17(d)
$$F = \overline{A}C\overline{D} + (\overline{B} + BC)D$$
$$= \overline{A}C\overline{D} + (\overline{B} + C)D$$
$$= \overline{A}C + \overline{B}D + CD$$

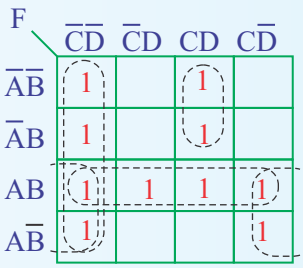


Q18.(b)

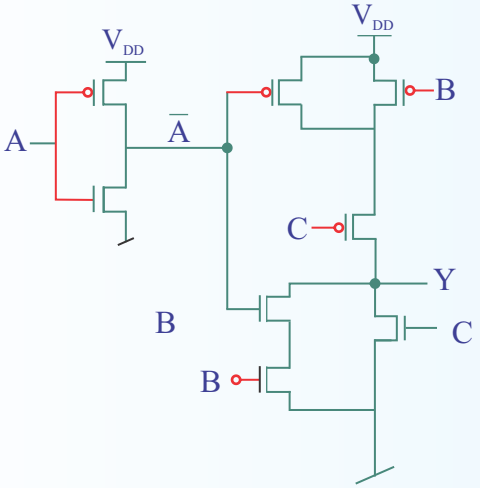
Input	PS	FF input	NS
A	Q	$D = out = \overline{A}D_0 + AD_1 = \overline{A}\overline{Q} + AQ$	Q^+
0	0	1	1
0	1	0	0
1	0	0	0
1	1	1	1



Q19.(b)
$$F = (\overline{A}\overline{D})C + (\overline{A}D)C + (A\overline{D}).1 + ADB$$
$$= \overline{A}\overline{C}\overline{D} + \overline{A}CD + A\overline{D} + ABD$$
Use K'map to get minimal SOP expression
$$F = \overline{A}CD + \overline{C}\overline{D} + AB + A\overline{D}$$



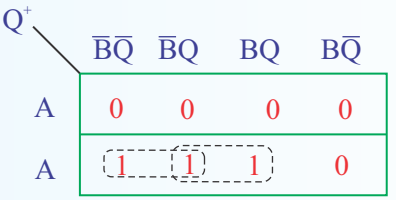
Q20



λ=4

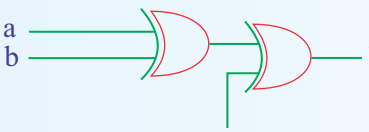
Q21.(d)

Inputs		PS	NS
A	B	Q	Q^+
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1



$Q^+ = A\bar{B} + AQ$

Q22.(d) *1.*



2.

$Y = A + (B \oplus C), B = C \Rightarrow B \oplus C = 0$

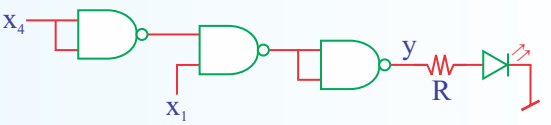
$Y = A \text{ while } B \neq C \Rightarrow B \oplus C = 1$

$Y = 1 + A = 1$

Q23.(b)

y	$\bar{x}_3\bar{x}_4$	$\bar{x}_3x_4$	x_3x_4	$x_3\bar{x}_4$
$\bar{x}_1\bar{x}_2$	0	0	0	0
$\bar{x}_1x_2$	0	0	0	0
x_1x_2	×	×	×	×
$x_1\bar{x}_2$	1	0	×	×

$y = x_1\bar{x}_4 = \overline{\overline{x_1\bar{x}_4}}$



Q24.(c) The circuit is designed to do the subtraction operation, that is, X – Y. For z = 1, $S_3S_2S_1S_0 = 0000$, that is, X – Y=0 or X = Y.

Q25.(b) Output frequency = f_{in} divided by 5×8×10=400.

$$\frac{f_{in}}{400} = 30 \times 10^3 \text{ and } f_{in} = 400 \times 30 \times 10^3 \text{ Hz} = 12MHz$$

Solutions
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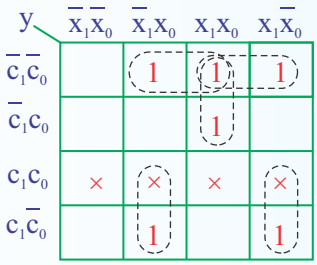
Q1.



Prime implicants are

$\bar{c}_1 x_1 x_0$, $\bar{c}_1 \bar{c}_0 x_0$, $\bar{c}_1 \bar{c}_0 x_1$,

$c_1 \overline{x_1} x_0$ and $c_1 x_1 \overline{x_0}$

$\lambda = 5$

Q2.(b) For $t_{dlly} = 0$ and considering only set up time constraints while ignoring hold time violations , the path from Q_1 to D_2 involves worst case delay $= 2 \times t_{d,max}$ of INV $+ t_{cq,max} + t_{su} = 2 \times 1 + 1 + 2 = 5$ns and there fore, the clock period $T_{CLK} \geq 5ns$.

$f_{CLK,max} = (1/5) \times 10^{-9}$ Hz $= 200\ MHz$.

The shortest delay from Q_2 to D_1 is $t_{cq,min}$ of FF2 $+ t_{d,min}$ of INV $= 0.5 + 0.5 = 1$ns. There fore , there is hold time violation at input D_1 of FF1 . While D_1 should be held constant for hold time , $t_h = 1.5$ns , Q_2 should not be allowed to arrive at D_1.

To eliminate this hold time violation at D_1, it is required to delay Q_2 at least by 0.5ns so that Q_2 arrives at D_1 at least after 1.5 ns. This can be achieved by delaying CLK to FF2 by 0.5ns. Thus, $t_{dly,min} = 0.5ns$.

Q3.(b)

8×1 MUX configuration gives

$$f = a + \bar{a}\bar{b}\bar{c} + \bar{a}b\bar{c} = a + \bar{a}\bar{c} = a + \bar{c}$$

$$f_1 = \bar{a} + a\bar{c} = \bar{a} + \bar{c} \neq f$$

$$f_2 = \bar{a}\bar{b}\bar{c} + \bar{a}b\bar{c} + a\bar{b} + ab = \bar{a}\bar{c} + a(b + \bar{b}) = a + \bar{c} = f$$

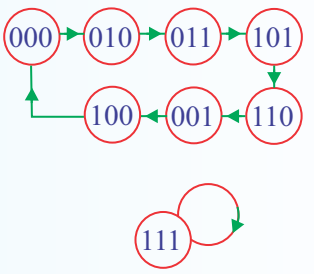
$$f_3 = a\bar{c} + \bar{a}c \neq f$$

$$f_4 = \bar{b}\bar{c} + b\bar{c} + \bar{a}bc = \bar{b}\bar{c} + b(\bar{c} + \bar{a}c) = \bar{b}\bar{c} + b(\bar{c} + \bar{a}) = (\bar{b} + b)\bar{c} + \bar{a}b = \bar{a}b + \bar{c} \neq f$$

Q4.(d) $01000\,11010_2 = 282_{10}$
and $v_0 = (5/1025) \times 282 = 1.3756\,V \neq 2.82\,V.$

Q5.(d)

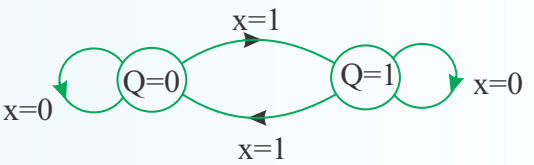
PS			FF	Inputs		NS		
Q_1	Q_2	Q_3	$D_1 = Q_3$	$D_2 = \overline{Q}_1\overline{Q}_3 + Q_1Q_3$	$D_3 = Q_2$	Q_1^+	Q_2^+	Q_3^+
1	1	1	1	1	1	1	1	1
0	0	0	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	0	0	1	0	0	1
0	0	1	1	0	0	1	0	0
1	0	0	0	0	0	0	0	0



The circuit is mod -7 counter without built in self-starting feature. From state $Q_1\,Q_2\,Q_3 = 111$, there is no ongoing.

Q6.(b)

PS	Input	FF Input		NS
Q	X	$S = X \oplus Q$	$R = \overline{X \oplus Q}$	Q^+
0	0	0	1	0
0	1	1	0	1
1	0	1	0	1
1	1	0	1	0



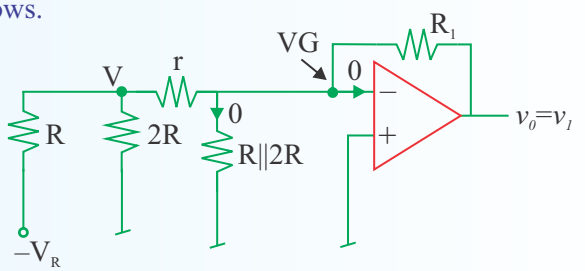
Q7. Let $v_0 = v_2$ for $b_3\,b_2\,b_1\,b_0 = 0100$ and $v_0 = v_1$ for $b_3b_2b_1b_0 = 0010$.
Then, $v_2 = 2\,v_1$ will ensure that circuit acts as a 4-bit DAC.
For $b_3b_2b_1b_0 = 0100$, $v_0 = v_2 = v_R \times (R_1/2R)$
For $b_3b_2b_1b_0 = 0010$, $v_0 = v_1$ is calculated as follows.

$$\frac{-V_R - V}{R} = \frac{V}{2R} + \frac{V}{r} \Rightarrow V = \frac{-2r\,V_R}{2R + 3r}$$

$$\frac{0 - v_1}{R_1} = \frac{V}{r} \Rightarrow v_1 = -\frac{R_1}{r}\left[\frac{-2rV_R}{2R + 3r}\right]$$

$$= \frac{2R_1V_R}{2R + 3r}$$

$$v_2 = 2v_1 \Rightarrow \frac{R_1V_R}{2R} = \frac{4R_1V_R}{2R + 3r} \Rightarrow \frac{r}{R} = k = 2$$



Q8. Step size, $S = 1.5/2^4 = 0.09375$V and $1.0/0.09375 = 10.66$.
One step below, $(10)_{10} = (1010)_2$ and digital reading $(1010)_2$ represents $10 \times 0.09375 = 0.9375$V. Error $= 1.0 - 0.9375 = 0.0625$V $= 62.5mV$.

Q9.(b) $f(a, b, c) = \overline{S_0}(\bar{a}\,b + a\,\bar{b}) + S_0\overline{(b + c)}$; $S_0 = a$

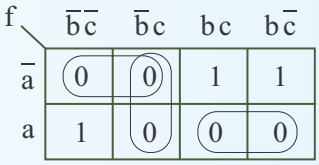
$= \bar{a}(\bar{a}\,b + a\,\bar{b}) + a\,\bar{b}\,\bar{c} = \bar{a}\,b + a\,\bar{b}\,\bar{c}$

Use K' map to get

$f' = \bar{a}\bar{b} + \bar{b}c + ab$

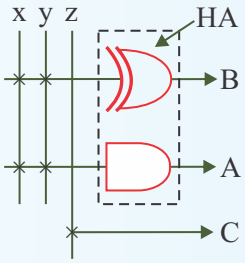
$f = (f')' = \overline{\bar{a}\bar{b} + \bar{b}c + ab}$

$= (a + b)(b + \bar{c})(\bar{a} + \bar{b})$



Q10.(c)

decimal	Inputs			Output		
d	x	y	z	A	B	C
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	0
3	0	1	1	0	1	1
4	1	0	0	0	1	0
5	1	0	1	0	1	1
6	1	1	0	1	0	0
7	1	1	1	1	0	1

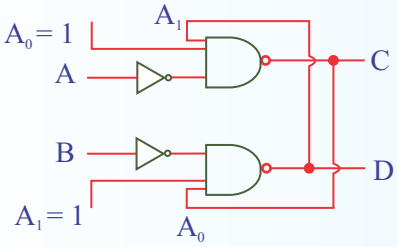


$A = xy$

$B = \bar{x}y + x\bar{y} = x \oplus y$

$C = z$

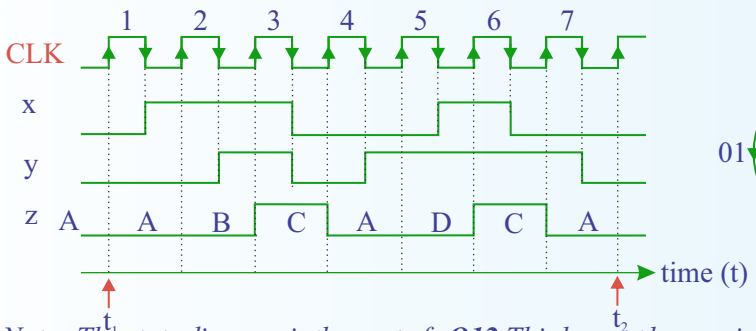
Q11.(c) The gate equivalent circuit is

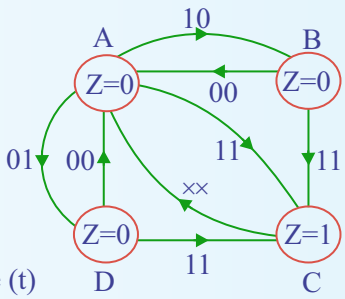


A	B	C^+	D^+	Action
0	0	C	D	no change
0	1	0	1	reset
1	0	1	0	set
1	1	1	1	invalid

S=A, R=B, Q=C and $\overline{Q} = D$

Q12.(b)





Note : The state diagram is the part of ***Q12****. This has not been printed in the book. Inconvenience is regretted.*

Q13.(c) A table of transition from Q (present state) to Q^+ (next state) as per inputs J and K of JK flip flop together with required T input of T flip flop for corresponding state transition , is demonstrated below.

J	K	Q	Q^+	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

$$T = \bar{J}KQ + J\bar{K}\bar{Q} + JK\bar{Q} + JKQ = (\bar{J}\bar{K}).0 + (\bar{J}K)Q + (J\bar{K})\bar{Q} + (JK).1$$

Also , $T = out = \bar{J}\bar{K}.I_0 + \bar{J}K.I_1 + J\bar{K}.I_2 + JK.I_3$

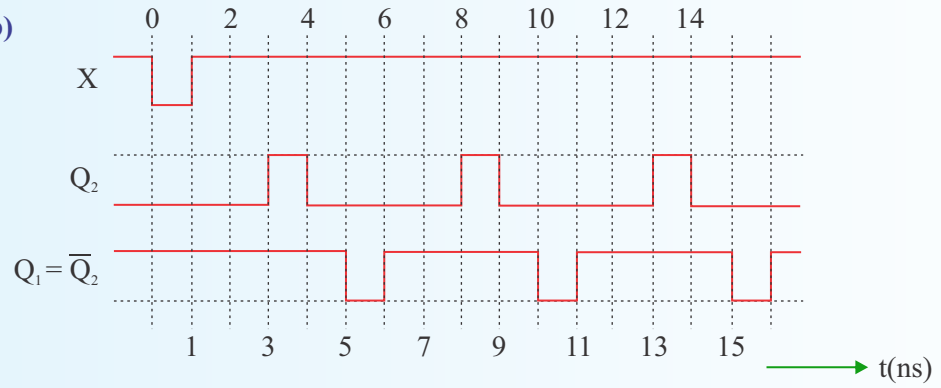
Compare to get $I_0 = 0, I_1 = Q, I_2 = \bar{Q}$ *and* $I_3 = 1$

Q14.(d) The design of NOR gate demands *4* PMOS transistors in series and *4* NMOS transistors in parallel .The on resistance of a MOSFET is inversely proportional to W/L ratio . Each PMOS transistors should have W/L ratio equal to *4p* so that the delay of NOR gate is equal to that of basic inverter .

The design of NAND gate demands *4* NMOS transistors in series and *4* PMOS transistors in parallel. In order that the delay of NAND gate is equal to that of basic inverter , the W/L ratio of each NMOS transistor should be *4n*.

In the basic CMOS inverter , the W/L ratio *'p'* of PMOS transistor is about 2 - 3 times the W/L ratio *'n'* of NMOS transistor so that the two transistors have equal on resistance. Therefore, the NOR gate requires the area much larger than the NAND gate.

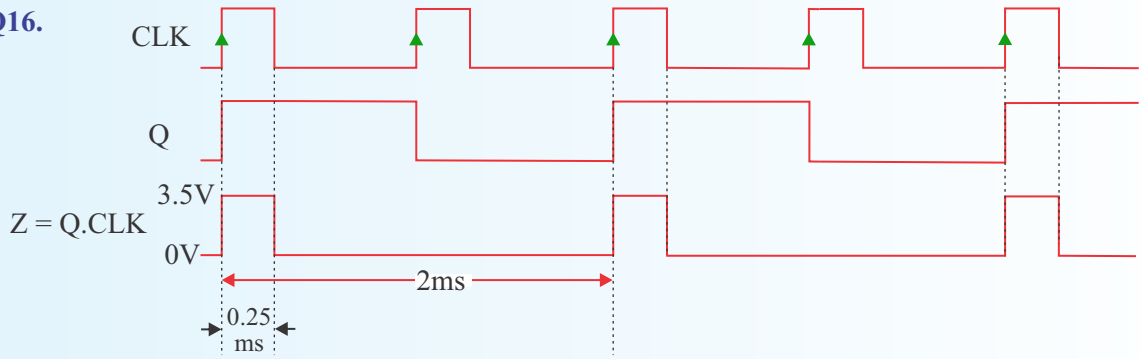
Q15.(b)



It is apparent from the waveforms sketched just above, that the outputs Q_1 and Q_2 are oscillatory in nature but the duty ratio at Q_1 is $(4/5) \times 100 = 80\%$ and that at Q_2 is $(1/5) \times 100 = 20\%$.
The average power dissipated in resistor $5k\Omega$ is

$$P_{av} = \text{Peak Power} \times (\text{duty cycle at } Q_1) = \frac{5^2}{5k\Omega} \times 0.8 = 4mW$$

Q16.



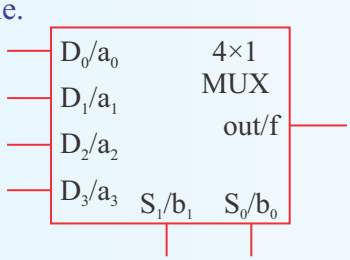
The waveform at node Z has duty cycle $= 0.25/2 = 0.125$
The average power dissipated in 360Ω resistor is $P_{av} = (3.5^2/360) \times 0.125\text{W} = 4.25mW$

Corrigendum:

In fig., the NAND gate should be AND gate . In answer key of Q16, read 4.25 instead of 8.5.Inconvenience is regretted

Q17.(c) $X = \overline{A}\,\overline{B}.0 + \overline{A}B.1 + A\overline{B}.0 + AB.A = AB + \overline{A}B = B$
$Y = \overline{C}X + C.C = B\overline{C} + C = B + C$

Q18.(c) The functionality is 4×1 MUX with b_1b_0 as select lines, a_0 to a_3 as data lines and f as output line.



Select Lines		Output
b_1	b_0	f
0	0	a_0
0	1	a_1
1	0	a_2
1	1	a_3

Q19.(a)

$$\phi(x_1, x_2, x_3) = x = x_1\overline{x}_2 + \overline{x}_1x_3$$

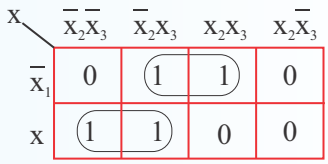
$$\phi(a, b, \overline{c}) = y_1 = a\overline{b} + \overline{a}\overline{c}$$

$$y_2 = \phi(y_1, a, \overline{b+\overline{c}}) = y_1\overline{a} + \overline{y}_1(\overline{b+\overline{c}})$$

$$= (a\overline{b} + \overline{a}\,\overline{\overline{c}})\overline{a} + \overline{a\overline{b}+\overline{a}\overline{\overline{c}}}.\overline{b}\overline{\overline{c}} = a\overline{c} + a\overline{b}.\overline{a}\overline{\overline{c}}.\overline{b}\overline{\overline{c}}$$

$$= a\overline{c} + (\overline{a}+b)(a+c)\overline{b}\overline{\overline{c}} = a\overline{c} + [a\overline{c} + ab + bc]\overline{b}\overline{\overline{c}} = a\overline{c} + a\overline{b}c$$

$$y = \overline{y_2.b + \overline{c}} = \overline{y_2}.\overline{b}\overline{\overline{c}} = \overline{(a\overline{c} + a\overline{b}c)}\overline{b}\overline{\overline{c}} = \overline{a\overline{b}c} = a + b + \overline{c}$$



$x = x_1\overline{x}_2 + \overline{x}_1x_3$

Q20.(d) $X = \overline{\bar{a}\bar{b}c}\ \overline{\bar{a}\bar{b}d}\ \overline{\bar{a}bd}\ \overline{\bar{a}bc} = a\bar{b}c + \bar{a}\bar{b}d + abd + abc$

X \	$\bar{c}\bar{d}$	$\bar{c}d$	cd	$c\bar{d}$
$a\bar{b}$	1	1		1
$\bar{a}b$				
ab		1	1	1
$a\bar{b}$				

The LED turns on when X = 0 and this is true *when input is greater than 2 but less than 13.*

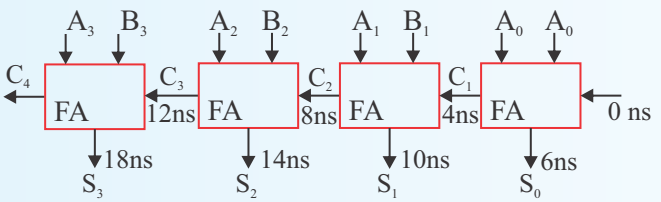
Decimal	a	b	c	d	X
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

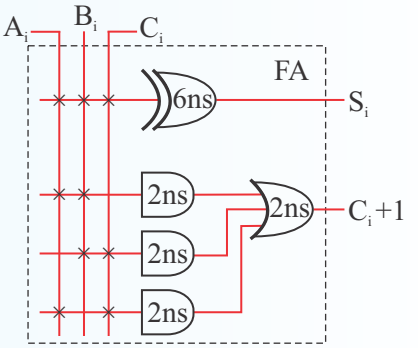
Q21.(b) $X = (a \oplus b)\overline{(b \oplus c)}c = (\bar{a}b + a\bar{b})(\bar{b}\bar{c} + bc)c$

$= (\bar{a}b + a\bar{b})bc = \bar{a}bc$

For *abc = 011*, the transistor terms on and so only the LED.

Q22. As demonstrated below, total time for a successful addition operation = *18ns.*



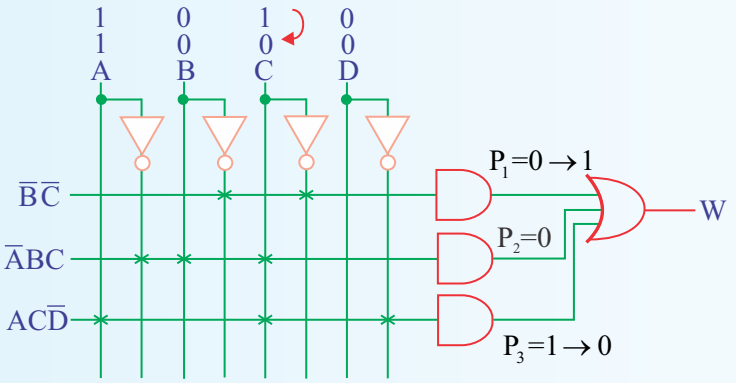


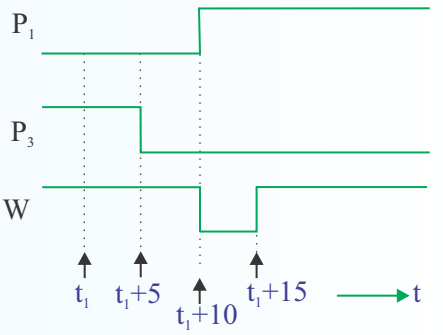
Q23.(d) $f = \bar{Z}D + ZB = \bar{Z}(\bar{X}Y + X\bar{Y}) + Z\bar{X}Y$

For Z = 1, f = 0 indicates either X = 0 and Y = 0 or X = 1 and Y = 0/1.

Q24.(d) In fact, the input x = 0111 is correctly matched to output y = *0011.*

Q25.(b) *The input C changes from 1 to 0 while inputs A, B and D remain unchanged.*





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